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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,740	03/03/2004	Sachiko Edo	Q80092	2870

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,740	EDO, SACHIKO	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 and 11-20 is/are rejected.

7)☒ Claim(s) 8-10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1- 20 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 03/03/2004.

3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. Claims 14-15, 19-20 provide for the use of a method of accessing a memory cell array, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is

indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claims 14-15,19-20 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd.* v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-7,11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwamoto et al. (U.S. Patent No. 5,592,434).

Regarding claim 1, Sato et al. disclose a synchronous type semiconductor memory device (Figure 1) comprising:

a memory cell array (1aa) in which memory cells are arranged in a matrix;

a row address decoder (2aa) which activates one of word lines in said memory ceil array based on a row address in response to a word activation signal;

a column decoder (4aa) which activates one of bit line pairs in said memory cell array based on a column address;

a sense amplifier (3aa) circuit which amplifies a voltage difference on said activated bit line pair in response to a sense amplifier activation signal;

a clock data storage section (9aa, 9ab) which stores clock data showing a frequency or period of an external clock signal (Column 6, lines 40-55, Figure 6); and

a control section (Figure 2) which generates said word activation signal based on a row address strobe signal, and generates said sense amplifier activation signal based on said clock data and said row address strobe signal in response to an internal clock signal synchronous with said external clock signal.

Regarding claims 2-7, Sato et al. disclose an operation timing signal generating section (Figure 2, 13) which receives said row address strobe signal. generates said word activation signal based on said row address strobe signal, and generates a plurality of candidate sense amplifier activation signals based on said row address strobe signal in response to said internal clock signal; and a selecting section (Figure 2, SEA) which selects one of said plurality of candidate sense amplifier activation signals as said sense amplifier activation signal based on said clock data, and wherein said operation timing signal generating section comprises: a buffer which receives said row address strobe signal, and outputs said word activation signal (Figure 2, 14); and a sequence of delay elements (Figure 4, 31) which shifts said row address strobe signal in response to said internal clock signal. and outputs said plurality of candidate sense amplifier activation signals from different ones of said delay elements, wherein each of

said delay elements is a flip-flop (Figure 9), and wherein at least one of said delay elements is triggered by a falling edge of said internal clock signal and remaining ones of said delay elements are triggered by a rising edge of said internal clock signal (Figure 10), and a data amplifier which amplifies and outputs data corresponding to the on said activated bit line amplified voltage difference pair in response to a data amplifier activation signal, section generates said data amplifier activation signal based on said clock data and a column address strobe signal in response to said internal clock signal (Figure2).

Regarding claims 12-13, 16-18, the apparatus discussed above would perform the method claims 12-13, 16-18.

Allowable Subject Matter

9. Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Sato et al. (U.S. Patent No. 5,892,730), and others, does not teach the claimed invention having a sequence of first delay elements which shifts said row address strobe signal in response to said internal clock signal. and outputs said plurality of candidate sense amplifier activation signals from different ones of said first delay

elements; and a sequence of second delay elements which shifts said column address strobe signal in response to said internal clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER